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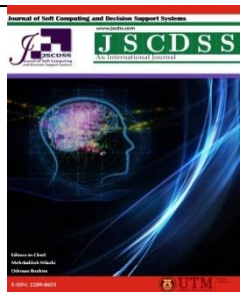

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4µW RMS-to-DC Converter in 180nm Technology Process for Biomedical Applications

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Abstract

This paper presents a low power RMS-to-DC converter for biomedical applications using CMOS transistors. This converter is designed by fewer number of transistors to reduce the power consumption as well as complexity so that only 18 transistors are included to build up the circuit. To make the circuit suitable for biomedical application, CMOS transistors operate in subthreshold region helping with reducing the power dissipation. This circuit takes the advantages of current-mode approach and translinear principle to make the circuit performance suitable for biomedical purposes and better than previous state-of-the-art works. Mathematical operations have been done for better understanding of the circuit operation. To verify the circuit performance, simulations have been done through H-spice in 180nm technology process to validate the analysis and topology of this converter. Based on the simulation results, the circuit has a low power of 4µW, low supply voltage of 0.9V, low relative error of 6%, bandwidth of 3 MHz, and input range of 50nA-450nA.

Keywords: RMS-to-DC converter, Subthreshold, MOS Translinear Loops (MTL)

1. Introduction

RMS-to-DC converter is an electronic circuit which is used for estimation of the average energy content in an electronic signal (Mulder et al., 1997; Mulder et al., 1996; Wey et al., 2000; Danesh et al., 2013). The converter is widely used in instrumentation devices (Haddad et al., 2003), biomedical ICs (Kafe et al., 2014), and syllabic companding systems (Frey et al., 200).

There are two approaches for designing RMS-to-DC converters: 1) current-mode approach, 2) voltage-mode approach. A current-mode circuit enables current processing and has certain essential advantages against a voltage-mode circuit such as wide bandwidth, high slew rate, low power consumption, and simple circuitry (Wilson, 1990; Toumazou et al., 1990), to name but a few. A squarer cell is an essential component in recent designed current-mode RMS-to-DC converters. The input range of two-quadrant squarer is wider than a one-quadrant one (Toumazou et al., 1990). The MOS translinear loops (MTL) derived by Seevinck and Wiegerink for the first time (Seevinck et al., 1991). MTL circuits are designed by applying the MTL principle and used in synthesizing many nonlinear signal processing functions (Mulder et al., 1996). The increasing demand for low-voltage/low-power integrated circuits has encouraged the conception of CMOS current-mode architectures. Up-down translinear loop in different computational circuits (Danesh et al., 2019; Lopez-Martin et al., 2003) and class-AB linear transconductors (Cruz-Blas et al., 2005) has been used. In (Danesh et al., 2019), the up-down structure of squarer cells uses no additional supply voltages and has less complexity. Also, the working region of transistors is weak inversion leading to less power consumption. From this point of view, the design process of low power actuators like reaction wheels (Izadi et al., 2015) is developed for reducing power consumption. In this paper, a two-quadrant low-power current-mode RMS-to-DC converter is presented which uses translinear principle with MOS transistors operating in weak inversion region. Due to the features of the current-mode structure used in this converter, the complexity and power consumption of the circuit are reduced. Power consumption and design simplicity are two significant features. The simplicity in the design process brings about more accurate fault detection model for sensors (Izadi et al., 2016; Izadi et al., 2019; Izadi et al., 2017). Therefore, circuit complexity should be considered in devices requiring low power consumption. For example, (Bellasi et al., 2013) proposes an Analog-to-Information Converter (AIC) based on compressive sensing which is more energy-efficient and faster than other state-of-the-art Analog-to-Digital Converters (ADC). Also, (Zanddizari et al., 2018) proposes a signal processing

algorithm to sense the biomedical signal in a very small size that enables the design to work faster with less power consumption for both sensing electrooculogram signals (Mitra et al., 2018) and magnetic resonance imaging MRI (Mitra et al., 2018). They use some post-processing to recover the quality of sensed signal in a remote server via Kronecker technique.

In this paper, a current-mode analog multiplier is presented that contains two squarer cells with MOS transistors operating in weak inversion region. The circuit take the advantage of a two-quadrant squarer cell which helps the circuit with increasing the input range in comparison with recent works. The squarer cell re-build the input signal to use it again in the converter. This technique makes the circuit more applicable as there is no need to apply another external input signal to the converter. Also, there is no additional power supplies to bias the transistors that helps the converter consumes les power dissipation. The simulation results indicate that the circuit performs perfectly with lower power consumption with lesser relative error. The remaining of the paper is organized as follows; In section 2, the principle operation of the circuit is explained and the circuit analysis is given in section 3. The simulation results of the proposed converter are presented in section 4 and the paper is concluded in section 5.

2. Principle operation of the converter

One of the most notable instances of nonlinear dynamic operation from a practical viewpoint is the RMS-to-DC conversion. In its basic form, and assuming input and output currents, such operation can be described as $I_{out} = \sqrt{< I_{out}^2 >}$, where I_{in} and I_{out} are the input and output currents of the RMS-to-DC converter, respectively, and the operator $<...>$ represents a time averaging. The equation presenting the output of current-mode RMS-to-DC converters, better in terms of offset (Mulder et al., 1996), is given by $I_{out} =< I_{in}^2 / I_{out} >$. Therefore, two operations have to be performed: squaring/division and subsequently, averaging. This converter is designed based on the block diagram proposed in (Danesh et al., 2013) and there is a feedback to use the output which is in DC format as a biasing current for the input transistors in the translinear loop.

3. Circuit analysis of the converter

The ratio of V/I for MOSFET transistors operating in the weak inversion region can be obtained from Eq. (1).

$$V_{GS} = \xi V_T Ln\left(\frac{I}{(W/L)I_{0n,p}}\right) \quad (1)$$

Except for ζ, Eq. (1) is similar to the exponential I_C / V_{BE} relationship in a bipolar transistor. The key point here is that as V_{GS} falls below v_{th}, the drain current drops at a finite rate. With typical values of ζ, at room temperature, V_{GS} must decrease by approximately 80mv for I_D to decrease by one decade based on Fig. 1. The squarer circuit performance is based on translinear loops including two NMOS and two PMOS transistors as shown in Fig. 2. The translinear loop used for the squarer cell is based on Up-Down structure which has been implemented by (Danesh et al., 2019) for designing RMS-to-DC converter and analog multiplier. This structure helps the circuit with reaching high linearity and bandwidth in spite of applying low current sources for biasing the transistors. Through analysis for four-transistor translinear loop in Fig. 2, it can be shown that (Danesh et al., 2013):

$$I_1.I_2 = I_3.I_4 \quad (3)$$

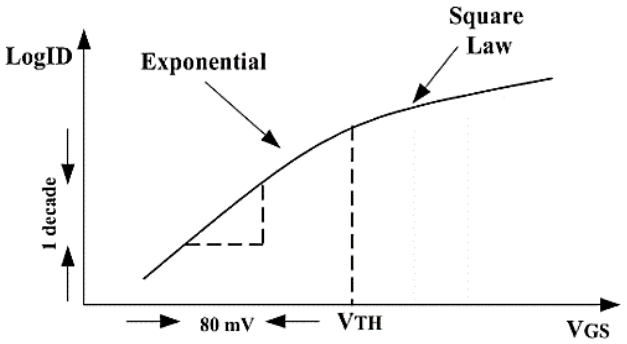

Fig. 1. MOS subthreshold characteristics.

The analysis for the proposed squarer circuit indicates that $I_1 = I_2 = I_{in}$ and $I_4 = I_{in} + I_3$. Thus, based on Eq. (3), I_3 can be given as:

$$I_3 = -\frac{1}{2}I_{in} + \frac{1}{2}\left(I_{in}^2 + 4I_B^2\right)^{0.5} \quad (4)$$

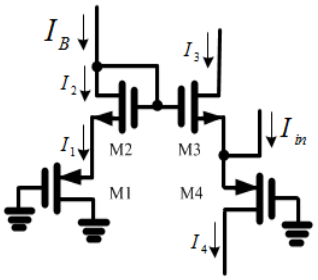

Fig. 2. Translinear loop of the squarer.

By applying power series for Eq. (4), I_3 can be re-written as:

$$I_3 = -\frac{1}{2}I_{in} + I_B + \frac{I_{in}^2}{8I_B} \quad (5)$$

For a good approximation, the value of the input current should be restricted to:

$$-2I_B \le I_{in} \le 2I_B \quad (6)$$

Combining equations $I_4 = I_{in} + I_3$ and Eq. (5), I_4 is equal to:

$$I_4 = +\frac{1}{2}I_{in} + I_B + \frac{I_{in}^2}{8I_B} \quad (7)$$

According to Eq. (5) and Eq. (7), if the circuit is able to remove bias current I_B and current $-0.5I_{in}$, it operates as a current squarer. Fig. 3 and Fig. 4 show the squarer and

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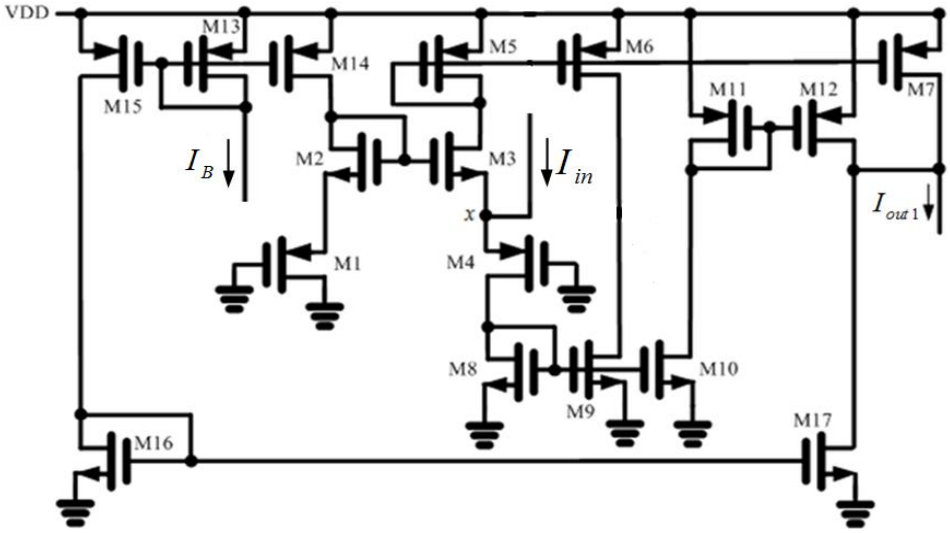

Fig. 3. The squarer circuit diagram.

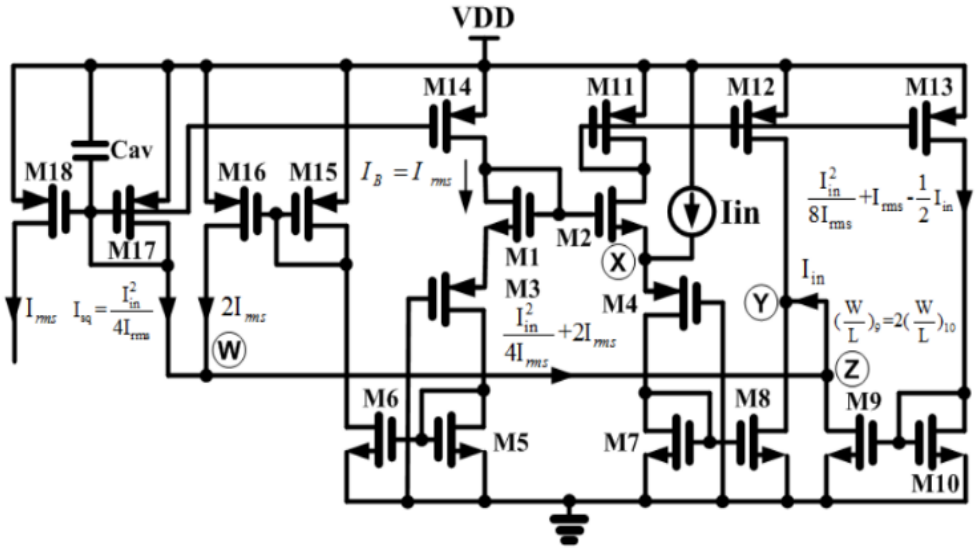

Fig. 4. The complete circuit diagram of the proposed RMS-to-DC converter.

complete circuit of the converter, respectively. According to Fig. 3 and Fig. 4, the transistor ration of M9 and M10 are equal to $(W/L)_9 = 2(W/L)_{10}$. Therefore, as $I_{16} = I_B = 2I_{rms}$, it can be shown that $I_9 = -I_{in} + 2I_{rms} + I_{in}^2 / I_{rms}$. Also, by writing equations for the current signals of M10-M13, we can show that the current of these transistors are equal to $-0.5I_{in} + I_{rms} + I_{in}^2 / I_{rms}$. Thereby, I_{in} can be given by subtracting I_{12} from I_8. Based on node W in Fig. 4, the squarer output current I_{sq} is equal to $I_{sq} = I_{in}^2 / I_{rms}$.

The input (I_{sq}) and output current (I_{out}) of a low pass filter can be written in Laplace and time domain as shown in Eq. (8).

$$\frac{I_{out}(s)}{I_{sq}(s)} = \frac{1}{1+\frac{s}{\omega_c}} \rightarrow I_{out}(s) + \frac{s}{\omega_c} I_{out}(s) = I_{sq}(s)$$
$$time\ domain \rightarrow \frac{1}{\omega_c}\frac{dI_{out}(t)}{dt} = I_{sq}(t) - I_{out}(t) \quad (8)$$

where ω_C is the filter cut-off frequency and the filter output current in Eq. (8) is equal to the current of M_{17}. Considering Eq. (8) in time domain and I/V equation of transistor 17, Eq. (8) can be re-written as:

$$\frac{dI_{out}}{dt} = \frac{I_{out}}{\xi V_T}\frac{I_C}{C} \Rightarrow \frac{1}{\omega_C}\frac{I_{out}}{\xi V_T}\frac{I_C}{C} = I_{sq}(t) - I_{out}(t) \quad (9)$$

According to $I_C(t) = I_{sq}(t) - I_{out}(t)$ and Eq. (9), the filter cut-off frequency is given by:

$$\omega_C = I_{out} / \xi V_T C \quad (10)$$

According to (Frey et al., 2004), the output ripple for such a circuit will be less than 1% of the converter output (I_{rms}), that is, the ripple output is small enough for biomedical applications. Therefore, based on Eq. (10), to have an error less than 1%, the low pass filter capacitor should be chosen as:

$$C \geq \frac{5I_{rms,MAX}}{\xi V_T (2\pi f_{\min})} \quad (11)$$

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where $f_{\min}$ is the lowest frequency which can be applied to the circuit. For example, if the sine input signal amplitude and frequency are equal to $I_M = 50nA$ and $f_{\min} = 100Hz$, respectively, to have a ripple error of less than 1%, the capacitance should be $C = 10nF$. With this capacitance, the ripple error for $I_M > 50nA$ is greater than 1%. In addition to this, to have a ripple error of less than 1% for $I_M < 450nA$ with the input frequency of 100Hz, the capacitance should be equal to $C = 80nF$ which occupies larger silicon area. According to Eq. (11), for achieving ripple error of less than 1%, the capacitance value decreases when frequency increases and the problem area appears for lower frequencies. Therefore, there is no necessity to choose C=80nF unless for special applications which require low input frequencies.

4. Simulation results

The performance of the circuit has been evaluated using simulations with H-spice in the 180nm technology process (see Table 1). The supply voltage and the low pass filter capacitor are equal to 0.9V and C=10nF, respectively. I_{rms}, the converter output, is shown in Fig. 5 and Fig. 6 for sine input signals having the same frequency of 100Hz with peak amplitudes of 450nA and 50nA, respectively. The relative error, calculated by Eq. (12), is depicted in Fig. 7 for different input signal amplitudes. The relative error of less than 4% is achieved for the input signal amplitudes ranging from 50nA to 450nA.

$$relative\ error = \left| \frac{I_{rms(True)} - I_{rms(Simulated)}}{I_{rms(True)}} \right| \times 100\% \qquad (12)$$

Simulation results show that the power consumption of the circuit for the maximum accepted input current (450nA) is 4μW.

Table 1
Simulation results of the converter.

Parameters	Result
Technology Process	180nm
Supply Voltage	0.9V
Power consumption	$4\mu A$
Circuit Complexity	6.0
Input range	50nA-450nA at 6% R.L

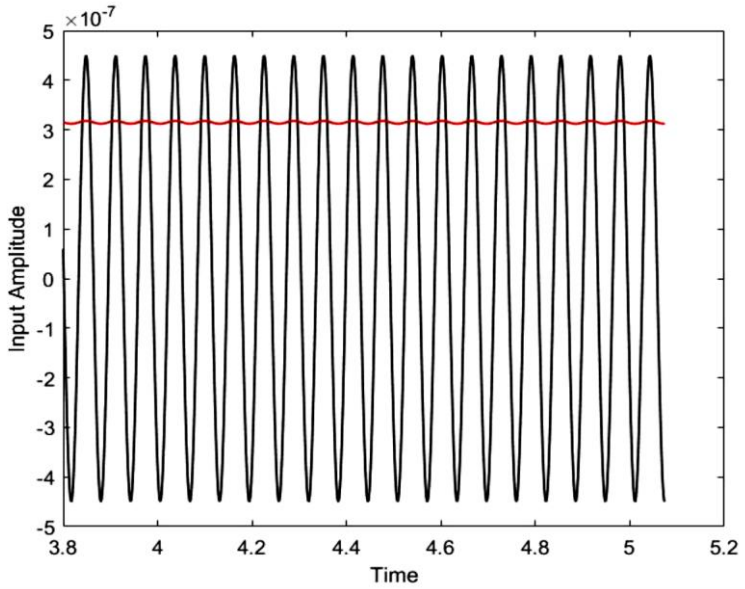

Fig. 5. Time response of output current of the converter for a sinusoidal input current with the peak amplitude of 450nA at frequency of 100Hz.

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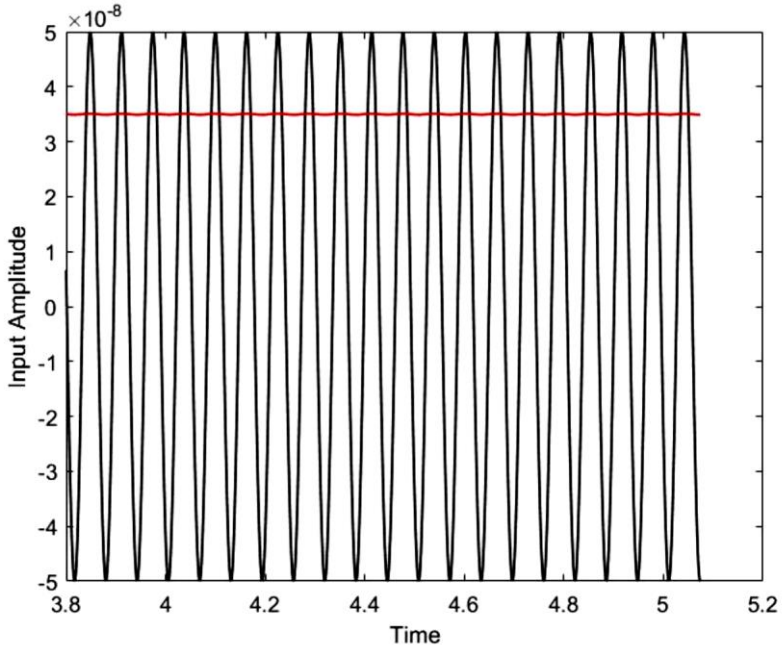

Fig. 6. Time response of output current of the converter for a sinusoidal input current with the peak amplitude of 50nA at frequency of 100Hz.

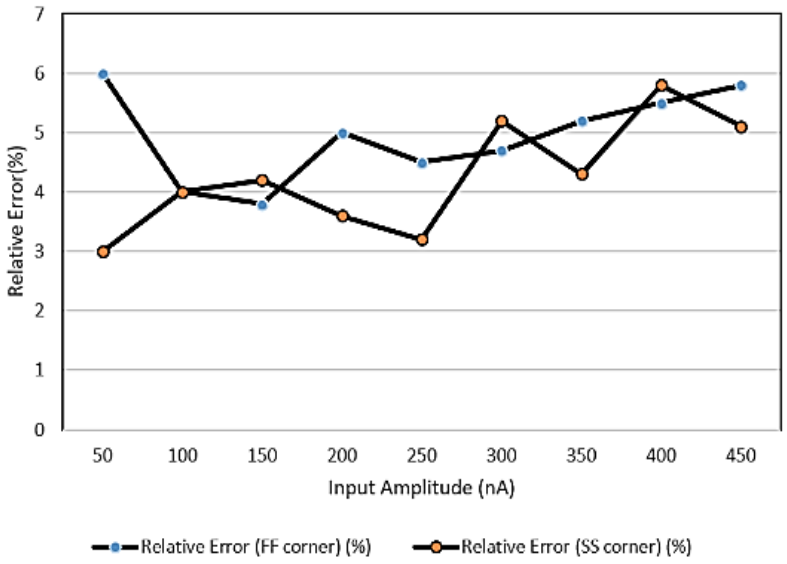

Fig. 7. Relative error vs. input current amplitude of the proposed converter.

5. Conclusion

In this paper, a very low-power, low-voltage two-quadrant current-mode RMS-to-DC converter based on MOS translinear principles operating in the weak inversion region was presented. We showed how the translinear loop can help with having less relative error for different input amplitudes. Mathematical equations have been provided for better understanding of the circuit performance, especially for the frequency analysis of averaging circuit. Simulation results confirmed the validity of circuit topology. The simulations were done for different input amplitudes to show and prove the input range of the converter. According to results, the converter has such a low power consumption of $4\mu W$ with supply voltage of 0.9V and wide input range of 50nA to 450nA. The relative error of this converter for corner cases indicates that the proposed circuit is not dependent on fabrication variations.

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