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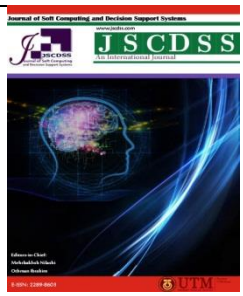

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Four-Quadrant Weak Inversion Analog Multiplier in the 180nm Technology for Biomedical Applications

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Abstract

In this paper, a current-mode four-quadrant analog multiplier circuit is proposed that utilizes MOS translinear principle. The parameters of TSMC 0.18µm technology are used to design the proposed multiplier that employs CMOS transistors operating in weak inversion region. The full combination of H-spice simulation, Monte Carlo simulation, L-edit post-layout simulation, and corner cases analysis are performed to prove its great merits of; low power consumption (1.5µW), low supply voltage (0.8V), body effect immunity, wide input range (±200nA), the bandwidth of 4.7 MHz, THD value lower than 2.8%, and the well-resistance of the proposed block against PVT (Technology Process, Supply Voltage, Temperature) non-idealises. The proposed architecture is compared with other current-mode week inversion multipliers indicating its noticeable superiorities over other ones particularly in FOM (Figure of Merits), consumed power and input range.

Keywords: Analog Multiplier, MOS Translinear, Monte Carlo, Weak Inversion

1. Introduction

Recently, the low-power low-voltage analog current-mode circuits have gained increasing attention. This attention is especially focused on the computing systems that prefer circuits with minimum consumed power and silicon area, wide dynamic range, and good linearity.

Power consumption is a subject that has been investigating by researchers in different areas of circuit designs from analog-to-digital convertors to many other parts of electronic circuits. Also, researchers try to find some signal processing approach to simplify computation, sensing, and manipulating electrical signals, particularly biomedical signals. Because for wearable biomedical sensors, we have limited power where we need both energy-efficient sensors and efficient signal processing approach. Hence designing a low power circuit may become a challenging issue. For example, recently very efficient approach for generating samples from an analog domain has been proposed based on compressive sensing (Bellasi et al., 2013). Also, in (Zanddizari et al., 2018) a post-processing method has been proposed based on Kronecker technique to accelerate the sampling phase of the analog-to-digital converters (Bellasi et al., 2013). This energy-efficient technique has been applied in two different classes of biomedical signals; electrocardiogram and magnetic resonance imaging signals (Mitra et al., 2018; Mitra et al., 2018), and the results show that both energy-efficient design and signal processing are required to achieve the ultimate goal of low power biomedical system. In (Ujan et al., 2016) they have used this idea for image enhancement, which can greatly benefit the biomedical field. The applications of such methods go beyond biomedical and to affect other fields of signal processing such as in (Khoshnevis and Ghorshi, 2019). There are also many other applications that energy-efficient circuits work along with an energy-efficient signal processing method.

Four-quadrant multiplication is one of the great important needed operations in analog computation and signal processing. It is used not only in mathematical operations but also in such applications as modulators, doublers, adaptive filters (SadoghiYazdi et al., 2010; Ndjountche et al., 1999), phase detection (Dash et al., 2012), mixers (Salama et al., 2003), neural networks (Spencer at al., 1994; Saxena et al., 1994), sensor applications (Blakiewicz et al.,2009), automatic gain controlling (Tacconi et al., 1993), fuzzy systems (Azeem et al., 2006; Afrang et al., 2010) and etc. Analog multiplier design was first reported in the work of Gilbert (Gilbert et al., 1968) which was implemented using BJT. Since then many works have been reported especially in CMOS technology (Chaisayun et al., 2012; popa et al., 2014; Al-Absi et al., 2013). The increasing demand for low voltage/low-power integrated circuits has encouraged the development of CMOS current-mode architectures. As in their voltage-mode counterparts, the operation principle of most available current-mode structures lays on drain current either deep in strong inversion (Leenaerts et al.,1996; Purushothaman et

al., 2008; Aksin et al., 2009) or in weak inversion region (Seevinck et al., 1991; Serrano-Gotarredona et al., 1999; Danesh et al., 2013). The advantage of (Danesh et al., 2013) is that the weak inversion area of CMOS transistors helps with consuming less power. But, the bandwidth gets reduced due to the fact that low current sources as the bias currents are used to bias the transistors. However, for biomedical purposes, such a disadvantage does not make any problems due to the fact that this application requires low bandwidths. In both cases, linearity becomes poorer as the amplitude of input signals increases. Based on the exponential characteristics of MOSFETs (in weak inversion region) or BJTs, four-quadrant current multiplier circuits have been designed from such different principles as stacked and folded MTL loops that the circuits need additional supply voltages and manufacture solutions for biasing and being immune from body effect, respectively (Al-Absi et al., 2013; Kasimis et al., 2011; Gravati et al., 2005; Mahmoudi et al., 2007). Therefore, the translinear loops such as Up-Down and class-AB can be implemented in order to relatively prevent the problems. The main reason for considering power consumption is the limited amount of battery sources. From this point of view, in modelling reaction wheel (Izadi et al., 2016; Izadi et al., 2017), the FET-based motor driver is considered as an optimized design.

In this paper, a current-mode four-quadrant multiplier is presented which contains three squarer cells and three translinear loops with MOS transistors operating in the weak inversion region, leading to very low power consumption. Nonetheless, using the weak inversion region of MOS transistors, bandwidth and input range would be decreased. However, being four-quadrant and using Up-Down (Nikseresht et al., 2017) and class-AB structures and unique priority of exponential applications compensate for the reduction of bandwidth and input range. One of the advantages of (Nikseresht et al., 2017) is that CMOS transistors which work in weak inversion region to reduce power consumption help with using the circuit as an on-chip module inside a biomedical integrated circuit. The design of this multiplier is such that other mathematical operations such as square-root, division, geometric mean, absolute value, and accumulation vector can be achieved due to hierarchical design which is based on the squarer circuit. Another advantage of this circuit is that it does not need additional supply voltage for biasing. Thereby, it can consume less power consumption compared to similar circuits. In addition, the up-down structure of translinear loops lead to the immunity of the circuit from body effect. The simulation results indicate that the circuit achieves very low power, low voltage, and wide input range. This work is organized as; in Section 2, principle operation of the proposed multiplier is presented. In Section 3, the squarer circuit will be analysed. Section 4 analyses the multiplier's circuit. Section 5 includes the complete simulation results about the operations of the proposed multiplier and comparison of results. Finally, the work is concluded in Section 6.

2. Principle operation of the proposed multiplier

The proposed block diagram of the multiplier circuit is shown in Fig. 1 (Danesh et al., 2019). (Danesh et al., 2019) proposes a novel architecture helping with increasing the bandwidth and the input range thanks to the reduction of parasitic capacitors. In addition, the structure proposed in (Danesh et al., 2019) reduces the circuit complexity bringing about less silicon area and power consumption since less number of transistors are used. According to this figure, multiplication operation is done by three squarer cells. I_{out} is the output current of the multiplier. I_B is DC bias current. I_x, I_y and $I_x + I_y$ are the input currents of squarer1, squarer2, and squarer3, respectively. The output current of this figure is calculated and shown in Eq. (1) and Eq. (2):

$$I_{sq1} + I_{sq2} + I_{out} = I_{sq3} \tag{1}$$

where I_{sq1}, I_{sq2} and I_{sq3} are the output currents of squarer1, squarer2 and squarer3, respectively.

$$\frac{I_x^2}{4I_B} + \frac{I_y^2}{4I_B} + I_{out} = \frac{(I_x + I_y)^2}{4I_B} \rightarrow I_{out} = \frac{I_x I_y}{2I_B} \tag{2}$$

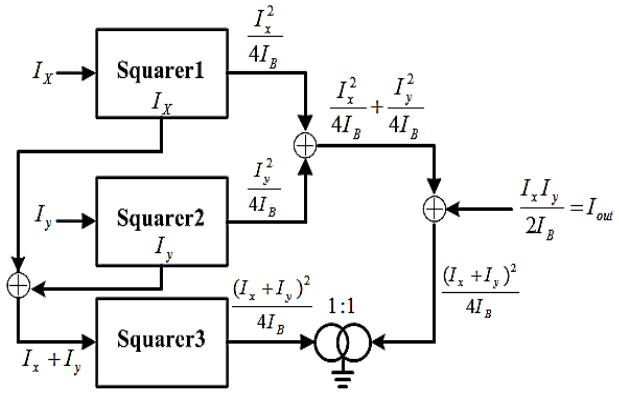

Fig. 1. Block diagram of the proposed multiplier.

3. Circuit analysis of the squarer cell

In the analysis of MOSFET, it is assumed that the devices turn off abruptly as V_{GS} drops below V_{th}. In reality, for $V_{GS} \approx V_{th}$, exists a weak inversion layer via which some current flows from D to S. Even for $V_{GS} < V_{th}$, I_D is finite, but it exhibits an exponential dependence on V_{GS}. This effect can be formulated as (Nikseresht et al., 2017):

$$I_D = I_0 . \frac{W}{L} . \exp \frac{V_{GS}}{\xi . V_T} \tag{3}$$

where $I_0 = I_S . e^{V_{th}/\xi V_T}$, $I_S = 2\xi . \mu . C_{ox} . V_T^2$, $V_T = kT/q$ and $\xi > 1$ is a non-ideal factor. Except for ξ, Eq. (3) is similar to the exponential I_C / V_{BE} relationship in a bipolar transistor. The key point here is that as V_{GS} falls below V_{TH}, the drain current drops at a finite rate. With typical values of ξ, at room temperature V_{GS} must decrease by approximately 80mV for I_D to decrease by one decade (Fig. 2) (Razavi et al., 2001; Enz et al., 1995). Principle operation of the squarer circuit is based on the translinear loop comprising two NMOS and two PMOS transistors shown in Fig. 3. This

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circuit is based on the up-down based topology using translinear loops. The advantage of this circuit is that it eliminates the body effect on the threshold voltage of the loop transistors. Therefore, it meets low supply voltages to be used for this structure, therefore this architecture is preferred to stacked mode (López-Martín et al., 2001).

According to Fig. 3, I_B, I_{in}, I_3 and I_4 are DC bias, input current and output currents, respectively. Since M1-M4 form a translinear loop, they follow the equations as (Seevinck et al., 1991):

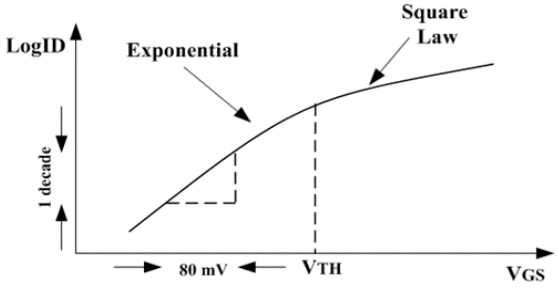

Fig. 2. MOS subthreshold characteristics.

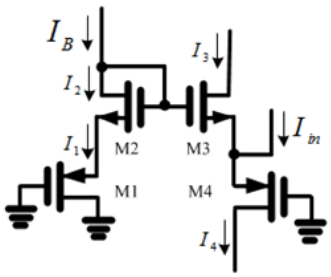

Fig. 3. Basic circuit of squarer cell (Danesh et al., 2019).

$$\sum_{CW} V_{GS} = \sum_{CCW} V_{GS}$$

$$\xi V_T \ln\left(\frac{I_1}{\left(\frac{W}{L}\right)_1 . I_0}\right) + \xi V_T \ln\left(\frac{I_2}{\left(\frac{W}{L}\right)_2 . I_0}\right) = \tag{4}$$

$$\xi V_T \ln\left(\frac{I_3}{\left(\frac{W}{L}\right)_3 . I_0}\right) + \xi V_T \ln\left(\frac{I_4}{\left(\frac{W}{L}\right)_4 . I_0}\right)$$

Assuming that $(W/L)_1 = (W/L)_4, (W/L)_2 = (W/L)_3$, Eq. (4) yields:

$$I_1 . I_2 = I_3 . I_4 \tag{5}$$

From the circuit analysis of Fig. 3, $I_1 = I_2 = I_B$ and $I_4 = I_{in} + I_3$, Eq. (6) gives as:

$$I_3^2 + I_{in} . I_3 - I_B^2 = 0 \tag{6}$$

Then solving quadratic Eq. (6), gives I_3 as:

$$I_3 = \frac{-I_{in} + \sqrt{I_{in}^2 + 4I_B^2}}{2} \tag{7}$$

Applying power series of Eq. (8) on Eq. (7) results to Eq. (9):

$$(1+x)^a = 1 + \sum_{n=1}^{\infty} C_n^a x^n, -1 < x < 1,$$
$$C_n^a = \frac{a(a-1)(a-2)...(a-n+1)}{n!} \tag{8}$$

$$I_3 = -\frac{1}{2} I_{in} + I_B + \frac{I_{in}^2}{8I_B} \tag{9}$$

where, for a good approximation, the value of the input current I_{in} should be restricted to:

$$-2I_B \le I_{in} \le 2I_B \tag{10}$$

Combining $I_4 = I_{in} + I_3$ and Eq. (9) provides:

$$I_4 = +\frac{1}{2} I_{in} + I_B + \frac{I_{in}^2}{8I_B} \tag{11}$$

According to Eq. (9) and Eq. (11), if the translinear circuit has the ability of removing I_B and $-1/2 I_{in}$, it operates as a current squarer, a key building block of the multiplier circuit. According to Fig. 4, the current of M5-M7 are equal to $-0.5I_{in} + I_B + I_{in}^2/8I_B$, $(W/L)_{17} = 2(W/L)_{16}$, and the current of M13-M16 are equal to $0.5I_{17} = I_B$. Thus, I_{in} can be extracted by subtracting I_6 from I_9 as shown in Eq. (12):

$$I_9 - I_6 = \frac{1}{2} I_{in} + I_B + \frac{I_{in}^2}{8I_B} - \left(-\frac{1}{2} I_{in} + I_B + \frac{I_{in}^2}{8I_B}\right) \tag{12}$$
$$= I_{in} = I_{out2}$$

Therefore, the output current of squarer cell is equal to:

$$I_{out1} = I_{sq} = I_7 + I_{12} - I_{17} = -\frac{1}{2} I_{in} + I_B + \frac{I_{in}^2}{8I_B} \tag{13}$$
$$+\frac{1}{2} I_{in} + I_B + \frac{I_{in}^2}{8I_B} - 2I_B$$

$$\rightarrow I_{out1} = I_{sq} = \frac{I_{in}^2}{4I_B} \tag{14}$$

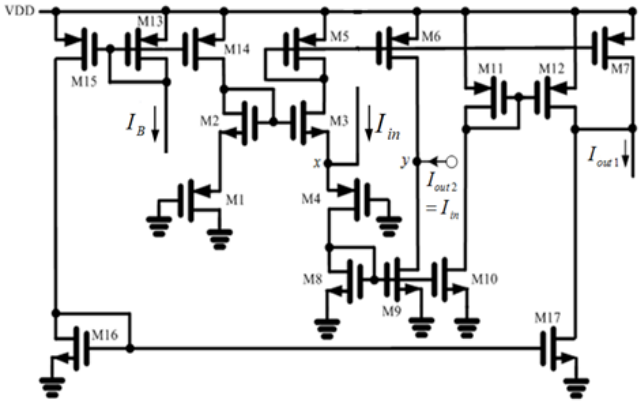

Fig. 4. The squarer cell used for the proposed analog multiplier.

Assuming the direction of the input signal of the squarer circuit is outward instead of inward, therefore $I_3 = I_{in} + I_4$. According to the final Eq. (5) for the translinear loop of

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constitutive circuit of the squarer cell, the quadratic equation is equal to:

$$I_3^2 - I_{in}.I_3 - I_B^2 = 0 \quad (15)$$

$$I_3 = +(1/2)I_{in} + I_B + (I_{in}^2/8I_B) \quad (16)$$

$$I_4 = -(1/2)I_{in} + I_B + (I_{in}^2/8I_B) \quad (17)$$

$$I_8 = I_9 = I_{10} = I_{11} = I_{12} = -0.5I_{in} + I_B + (I_{in}^2/8I_B) \quad (18)$$

$$I_5 = I_6 = I_7 = +(1/2)I_{in} + I_B + (I_{in}^2/8I_B) \quad (19)$$

Considering $I_{17} = 2I_B$, Eq. (13) and Eq. (18) to Eq. (19), it can be shown that $I_{out1} = I_{sq} = I_{in}^2/4I_B$. Therefore, this squarer performs as a two-quadrant circuit.

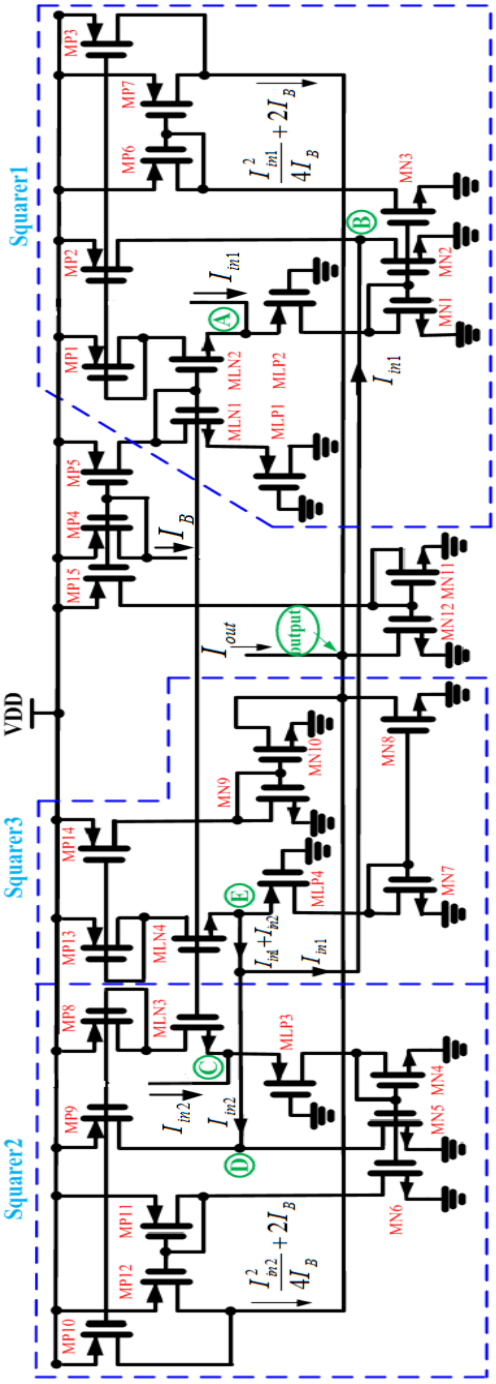

Fig. 5. Complete circuit diagram of the proposed multiplier.

4. Multiplier circuit analysis

As mentioned in sec. 2, the proposed multiplier is completed by 3 squarer cells, the circuit of which is shown in Fig. 4. The complete circuit diagram of the proposed multiplier is shown in Fig. 5. According to Fig. 5, the input currents I_{in1} and I_{in2} enter node A and C, respectively. The input current of squarer3 which is the summation of the extracted currents I_{in1} and I_{in2} from node B and D enters node E. Output currents of squarer1, squarer2 and squarer3 are equal to:

$$I_{sq1} = 2I_B + \frac{I_{in1}^2}{4I_B} \quad (20)$$

$$I_{sq2} = 2I_B + \frac{I_{in2}^2}{4I_B} \quad (21)$$

$$I_{sq3} = 2I_B + \frac{(I_{in1}+I_{in2})^2}{4I_B} \quad (22)$$

According to Fig. 5, the aspect ratio of transistors M4-M5, M15, and M12 are equal to $0.5(W/L)_{MN13}$. Therefore, the currents of MN8 and MN10 will be equal to:

$$I_{MN8} = \frac{1}{2}(I_{in1}+I_{in2}) + I_B + \frac{(I_{in1}+I_{in2})^2}{8I_B} \quad 23)$$

$$I_{MN10} = -\frac{1}{2}(I_{in1}+I_{in2}) + I_B + \frac{(I_{in1}+I_{in2})^2}{8I_B} \quad (24)$$

Using KCL at output node offers I_{out} as:

$$I_{out} = I_{MN10} + I_{MN8} + I_{MN12} - I_{sq1} - I_{sq2} \quad (25)$$

$$I_{sq3} = 2I_B + \frac{(I_{in1}+I_{in2})^2}{4I_B}$$

$$= 2I_B + \frac{I_{in1}^2}{4I_B} + \frac{I_{in2}^2}{4I_B} + \frac{I_{in1}.I_{in2}}{2I_B}$$

$$\rightarrow I_{out} = -\frac{1}{2}(I_{in1}+I_{in2}) + I_B + \frac{(I_{in1}+I_{in2})^2}{8I_B}$$

$$+\frac{1}{2}(I_{in1}+I_{in2}) + I_B + \frac{(I_{in1}+I_{in2})^2}{8I_B}$$

$$+2I_B - 2I_B - \frac{I_{in1}^2}{4I_B} - 2I_B - \frac{I_{in2}^2}{4I_B}$$

$$\rightarrow I_{out} = \frac{I_{in1}.I_{in2}}{2I_B} \quad (26)$$

It should be noted that DC terms of Eq. (20) to Eq. (22) does not need to be omitted. This was shown in Eq. (25) to Eq. (26), explicitly.

5. Simulation results

The performance of the circuit has been studied through simulation results using, MOS transistor provided by the 180nm CMOS TSMC process HSPICE and L-edit software. The supply voltage and power dissipation are 0.8V and

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1.5µW, respectively. To bias the devices in weak inversion region, the bias current is set to 200nA. The dc transfer characteristic curves of the multiplier are shown in Fig. 6 and Fig. 7. Both I_{in1} and I_{in2} are between $\pm$ 200nA. According to Eq. (8) to Eq. (10), to have less distortion, the maximum amplitudes of the input signals should be equal to 200nA.

Fig. 8 shows the application of the proposed multiplier as an amplitude modulator. The modulation is performed when I_{in1} and I_{in2} are the input signals which have the amplitude of 400nAp-p and the frequency of 100 KHz and 10 KHz, respectively. Also, the proposed circuit can operate as a frequency doubler when both I_{in1} and I_{in2} with the amplitudes of 200nA at 100 KHz frequency are applied. The output of the frequency doubler is shown in Fig. 9.

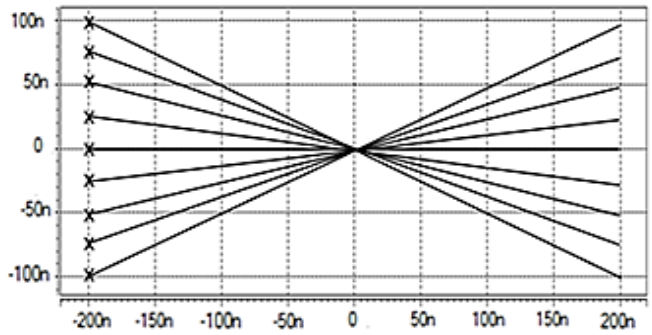

Fig. 6. The dc transfers characteristic curves versus I_{in1} .

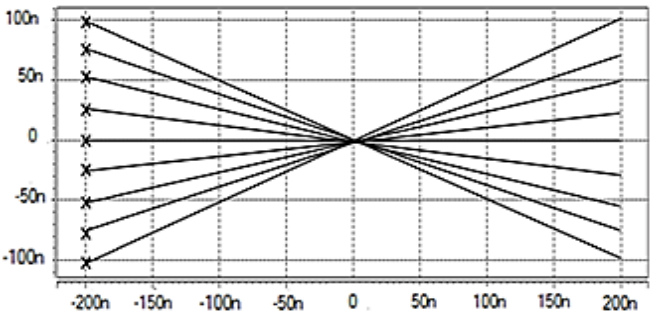

Fig. 7. The dc transfers characteristics curves versus I_{in2} .

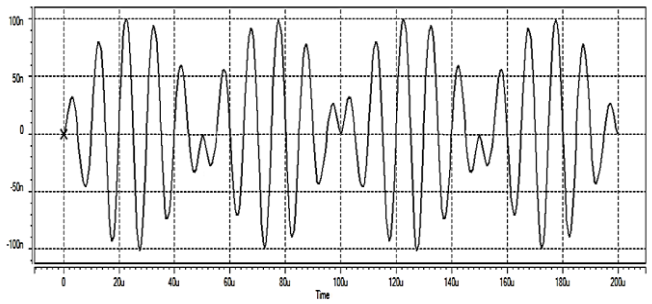

Fig. 8. Multiplication performance of the multiplier.

Fig. 10 and Fig. 11 show frequency responses of the output current I_{out} versus the input currents. Where a dc current of 200nA is applied to I_{in2} while I_{in1} is a sine signal with a variable frequency. The -3db bandwidth is approximately 5.2 MHz for both Fig. 10 and Fig. 11.

Multiplier non-linearity is calculated as shown in Eq. (27). The simulated non-linearity of the circuit is 2.7%.

$$Nonlinearity = \frac{\text{simulated output - theorical output}}{\text{p-p output simulated}} \times 100\% \quad (27)$$

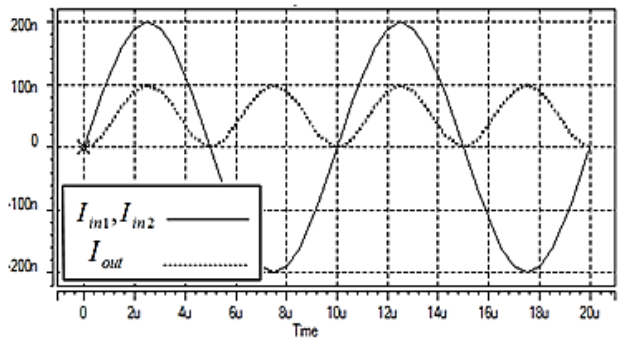

Fig. 9. The operation of the proposed circuit as a frequency doubler.

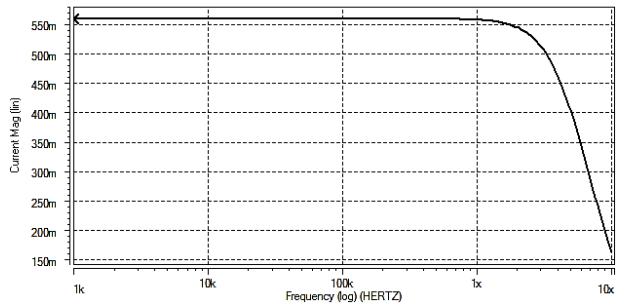

Fig. 10. Frequency response of I_{out} / I_{in1} .

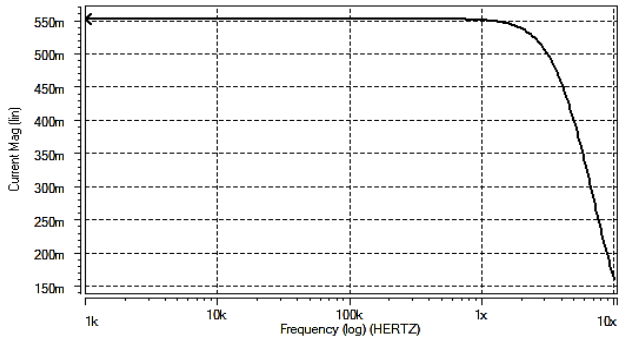

Fig. 11. Frequency response of I_{out} / I_{in2} .

The simulated results for THD indicate that THD value is less than 2.1% for the input amplitude of 200nA at the frequency of 50KHz. Fig. 12 shows THD of the proposed circuit for different input amplitudes at two different frequencies of 50 KHz and 100 KHz.

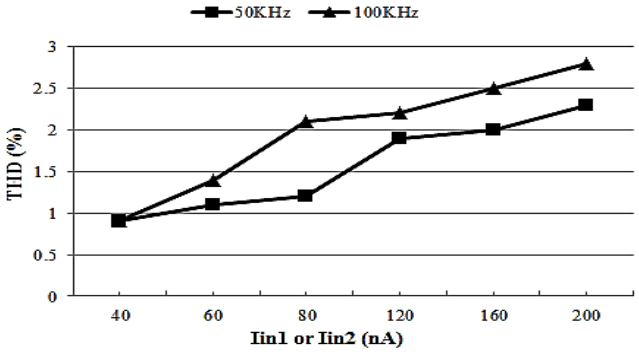

Fig. 12. THD of the circuit for different input amplitudes at two frequencies of 50KHz and 100KHz.

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Multiplication performance of the multiplier for corner cases of FF, SS, SF and FS are checked and shown in Fig. 13 to Fig. 16, respectively. These simulations have been achieved for $I_{in1} = 200^{nA}\sin(2\pi \times 250^{KHz})$ and $I_{in2} = 200^{nA}\sin(2\pi \times 100^{KHz})$.

FoM (Figure of Merits) contains important circuits' parameters like bandwidth, input range, power consumption and THD. Eq. (28) shows FoM calculation based on these parameters.

$$FOM = \frac{\text{Bandwidth(MHz)}\times\text{Input Range(nA)}}{\text{Power Consumption}(\mu\text{W})\times\text{THD}(\%)} \quad (28)$$

Calculated FOM for the proposed multiplier is 211 that shows a better value in comparison to other multipliers. Monte Carlo analysis is also performed while W, L, V_{th} and t_{ox} of all transistors change randomly as much as 2% with a standard deviation of 3 and simulations are repeated 50 times. Table 1 shows a comparison between the characteristics of pre and post layout simulation.

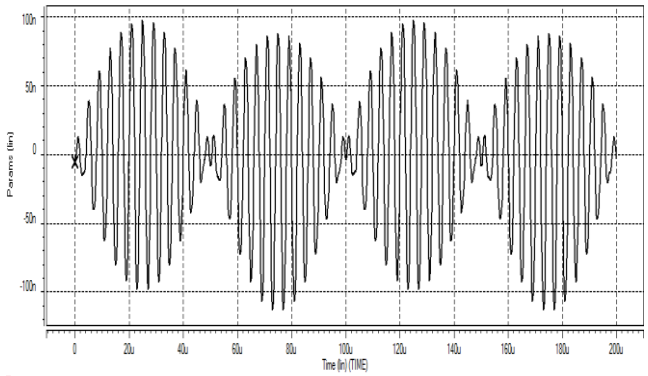

Fig. 13. Multiplication performance of the multiplier for FF corner case.

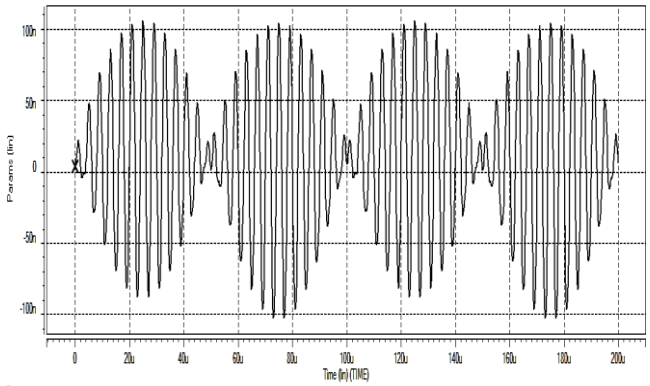

Fig. 14. Multiplication performance of the multiplier for SS corner case.

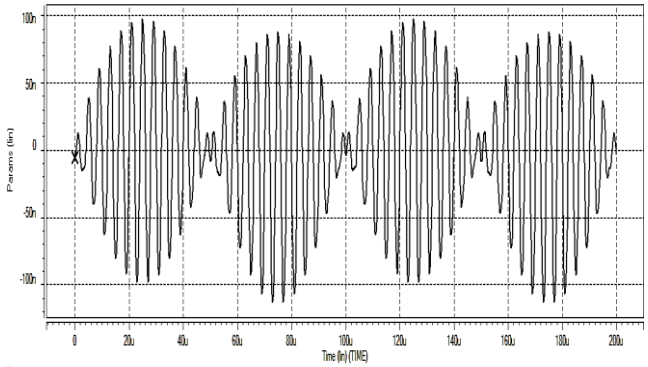

Fig. 15. Multiplication performance of the multiplier for SF corner case.

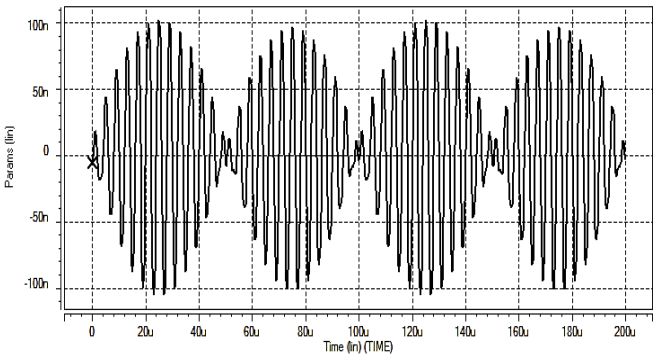

Fig. 16. Multiplication performance of the multiplier for FS corner case.

Table 1
Comparison of the multiplier's characteristics for pre and post layout simulations.

Parameters	Simulation	Post Layout
Technology Process(µm)	0.13	0.35
Supply Voltage	0.65	2
Bias Current (nA)	0.5	250
Input range (nA)	±4	±250
Nonlinearity (%)	NA	5
THD (%)	3.1@ 2KHz-0.1pA	0.9@ 1KHz-190nA
-3dB Bandwidth	NA	200KHz
Power Consumption	6.43nW	5.5µW
FoM	NA	10

Fig. 17 and Fig. 18 show Monte Carlo analysis of frequency and time responses for $I_{in1} = 200^{nA}\sin(2\pi \times 100^{KHz})$ and $I_{in2} = 200^{nA}$, respectively. According to these simulations, the proposed circuit sensitivity to technology process variations is low.

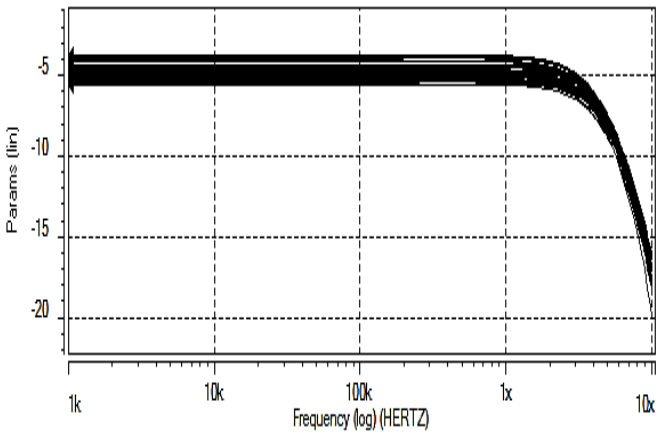

Fig. 17. Monte Carlo analysis of frequency response.

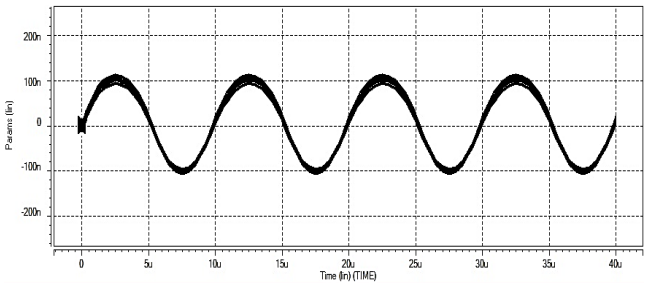

Fig. 18. Monte Carlo analysis of time response.

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Table 2
The comparison with the-the-state-of-art works.

Parameters	Purushothaman et al. (2008) (Simulation)	Aksin et al. (2009) (Experiment)	Seevink et al. (1991) (Simulation)	Afrang et al. (2010) (Simulation)	Mahmoudi et al. (2007) (Simulation)	This work (Simulation)
Technology Process(µm)	0.13	0.35	0.35	0.35	0.18	0.18
Supply Voltage	0.65	2	2	±0.75	1	0.8
Bias Current (nA)	0.5	250	50	50,100	100	200
Input range (nA)	±4	±250	±100	±30	NA	±200
Nonlinearity (%)	NA	5	2.8	0.3	0.88	3.3
THD (%)	3.1@ 2KHz-0.1pA	0.9@ 1KHz-190nA	1@ 100KHz-100nA	1.1@ 35nA	1.3@ 50KHz-100nA	2.8@ 50KHz-200nA
-3dB Bandwidth	NA	200KHz	19MHz	2.3MHz	0.768 MHz	4.7 MHz
Power Consumption	6.43nW	5.5µW	9 µW	2.3 µW	1.12 µW	1.5 µW
FoM	NA	10	211	28	211	224

6. Conclusion

In this paper, a very low-power, low-voltage four-quadrant current-mode multiplier based on MOS translinear loops operating in weak inversion is presented. Table 2 shows a comparison between our results and the results gathered from several state of the art studies. The proposed multiplier has many applications for a wide range of analog signal processing. Simulation results have been given to confirm the validity of the theoretical analysis. Carlo simulations were done to verify that the circuit performance is not dependant to process variations. The circuit operates by a low supply voltage of 0.8 bringing about a power consumption of 1.5µW. We verified that the power consumption of the circuit can be reduced more with the help of transistors working in weak inversion. The circuit takes the advantages of translinear loop which helps the circuit to perform with a low THD. In addition, we showed that the circuit achieves a high input range and bandwidth by using up-down structure.

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